

What is claimed is:

1 1. A test device for detecting whether the
2 alignment of bit line contacts and active areas in DRAM
3 devices is normal, wherein the test device is disposed in
4 a scribe line region of a wafer, comprising:

5 a bar-type active area, disposed in the scribe line,
6 having a center;

7 a bit line contact disposed on the center of bar-
8 type active area;

9 a bit line having a center coupled to the bit line
10 contact, and a first terminal and a second
11 terminal, wherein the bit line is essentially
12 perpendicular to the bar-type active area; and

13 two plugs disposed on the first terminal and the
14 second terminal of the bar-type active area
15 respectively, wherein the two plugs are
16 electrically coupled to the first terminal and
17 the second terminal of the bar-type active area
18 respectively.

1 2. The test device as claimed in claim 1, further
2 comprising two word lines disposed above two sides of the
3 bar-type active area respectively, and the two word lines
4 are essentially parallel to each other.

1 3. The test device as claimed in claim 1, wherein
2 a first resistance is detected by the first terminal of
3 the bit line and one of the two plugs, and a second
4 resistance is detected by the second terminal of the bit
5 line and the other of the two plugs, the alignment of the

6 bit line contact and the bar-type active area is
7 abnormal.

1 4. A method for detecting whether the alignment of
2 bit line contacts and active areas in DRAM devices is
3 normal, comprising:

4 providing a wafer with at least one scribe and at
5 least one memory area;

6 forming a plurality of memory cells in the memory
7 area and at least one test device in the scribe
8 line simultaneously, wherein the memory area
9 has bit line contacts and active areas, the
10 test device including:

11 a bar-type active area disposed in the scribe
12 line, having a center;

13 a bit line contact disposed on the center of
14 bar-type active area;

15 a bit line having a center coupled to the bit
16 line contact, and a first terminal and a
17 second terminal, wherein the bit line is
18 essentially perpendicular to the bar-type
19 active area; and

20 two plugs disposed on the first terminal and
21 the second terminal of the bar-type active
22 area respectively, wherein the two plugs
23 are electrically coupled to the first
24 terminal and the second terminal of the
25 bar-type active area respectively;

26 detecting a first resistance by the first terminal
27 of the bit line and one of the two plugs;

28 detecting a second resistance by the second terminal
29 of the bit line and the other of the two plugs;
30 determining whether the alignment of the bit line
31 and the bar-type active area of the test device
32 is normal according to the first resistance and
33 the second resistance; and
34 determining whether the alignment of the bit line
35 contacts and the active areas in the memory
36 areas is normal according to whether the
37 alignment of the bit line contact and bar-type
38 active area of the test device.

1 5. The method as claimed in claim 4, wherein the
2 test device further comprises two word lines disposed
3 above two sides of the bar-type active area respectively,
4 and the two word lines are essentially parallel to each
5 other.

1 6. The method as claimed in claim 4, wherein the
2 alignment of the bit line contact and the bar-type active
3 area is abnormal if the first resistance is not equal to
4 the second resistance.

1 7. A method for detecting whether the alignment of
2 bit line contacts and active areas in DRAM devices is
3 normal, comprising:

4 providing a wafer with at least one scribe and at
5 least one memory area;
6 forming a plurality of memory cells in the memory
7 area and at least one test device in the scribe
8 line at the same time, wherein the memory area

9 has bit line contacts and active areas, the
10 test device including:
11 a bar-type active area disposed in the scribe
12 line, having a center, a predetermined
13 width, and a predetermined resistivity;
14 a bit line contact disposed on the center of
15 bar-type active area;
16 a bit line having a center coupled to the bit
17 line contact, and a first terminal and a
18 second terminal, wherein the bit line is
19 essentially perpendicular to the bar-type
20 active area; and
21 two plugs disposed on the first terminal and
22 the second terminal of the bar-type active
23 area respectively, wherein the two plugs
24 are electrically coupled to the first
25 terminal and the second terminal of the
26 bar-type active area respectively;
27 detecting a first resistance by the first terminal
28 of the bit line and one of the two plugs;
29 detecting a second resistance by the second terminal
30 of the bit line and the other of the two plugs;
31 determining whether the alignment of the bit line
32 and the bar-type active area of the test device
33 is normal according to the first resistance and
34 the second resistance; and
35 determining whether the alignment of the bit line
36 contacts and the active areas in the memory
37 areas is normal according to whether the

38 alignment of the bit line contact and bar-type
39 active area of the test device.

1 8. The method as claimed in claim 7, wherein the
2 alignment of the bit line contact and the bar-type active
3 area is abnormal if the first resistance is not equal to
4 the second resistance.

1 9. The method as claimed in claim 8, further
2 comprising a step of determining the alignment shift of
3 the bit line contact and the bar-type active area
4 according to the first resistance, the second resistance,
5 the predetermined width and the predetermined
6 resistivity.

1 10. The method as claimed in claim 9, wherein the
2 alignment shift (ΔL) is determined by an equation:

3
$$\Delta L = W \times \frac{R_1 - R_2}{2R_{AA}};$$

4 wherein R_1 is the first resistance, R_2 is the second
5 resistance, R_{AA} is the predetermined resistivity and W is
6 the predetermined width.